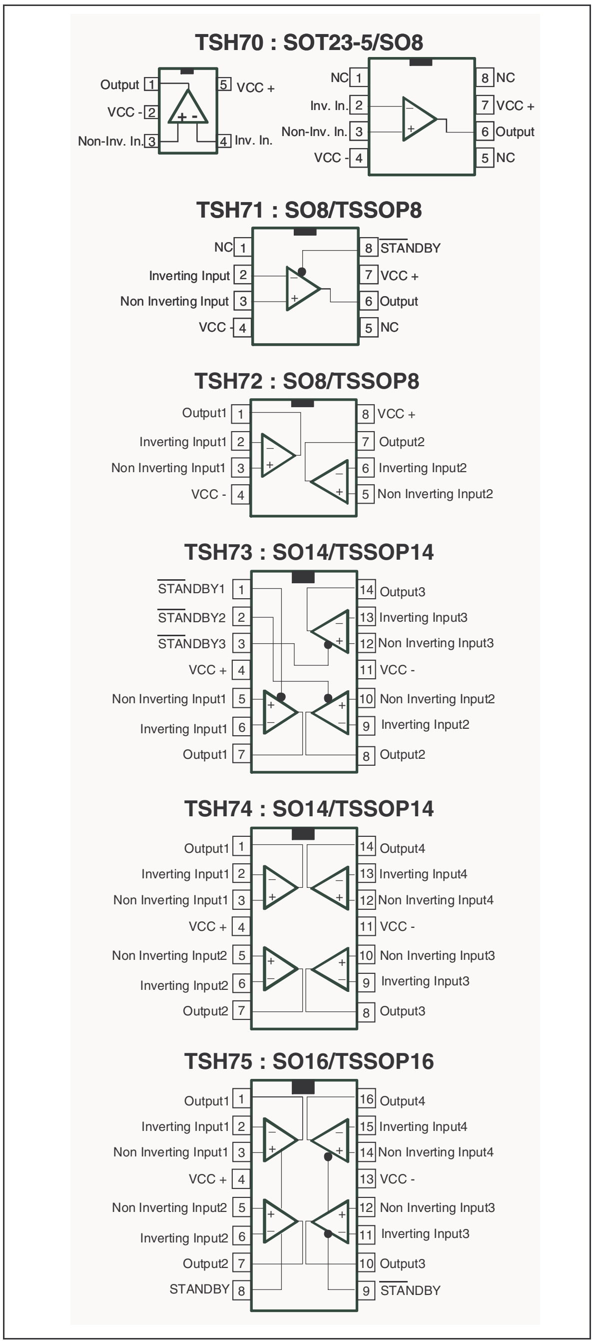
TSH70,71,72,73,74,75

Rail-to-Rail, Wide-Band, Low-Power Operational Amplifiers

- 3V, 5V, ±5V specifications
- 3dB bandwidth: 90MHz
- Gain bandwidth product: 70MHz
- Slew rate: 100V/ms
- Output current: up to 55mA
- Input single supply voltage
- Output rail-to-rail
- Specified for 150Ω loads
- Low distortion, THD: 0.1%
- SOT23-5, TSSOP and SO packages

Pin Connections (top view)



Description

The TSH7x series offers single, dual, triple and quad operational amplifiers featuring high video performances with large bandwidth, low distortion and excellent supply voltage rejection.

Running with a single supply voltage from 3V to 12V, these amplifiers feature a large output voltage swing and high output current capable of driving standard 150Ω loads. A low operating voltage makes TSH7x amplifiers ideal for use in portable equipment.

The TSH71, TSH73 and TSH75 also feature standby inputs, each of which allows the op-amp to be put into a standby mode with low power consumption and high output impedance. This function allows power saving or signal switching/multiplexing for high-speed applications and video applications.

To economize both board space and weight, the TSH7x series is proposed in SOT23-5, TSSOP and SO packages.

Applications

- Video buffers
- ADC driver
- Hi-fi applications

1 Order Codes

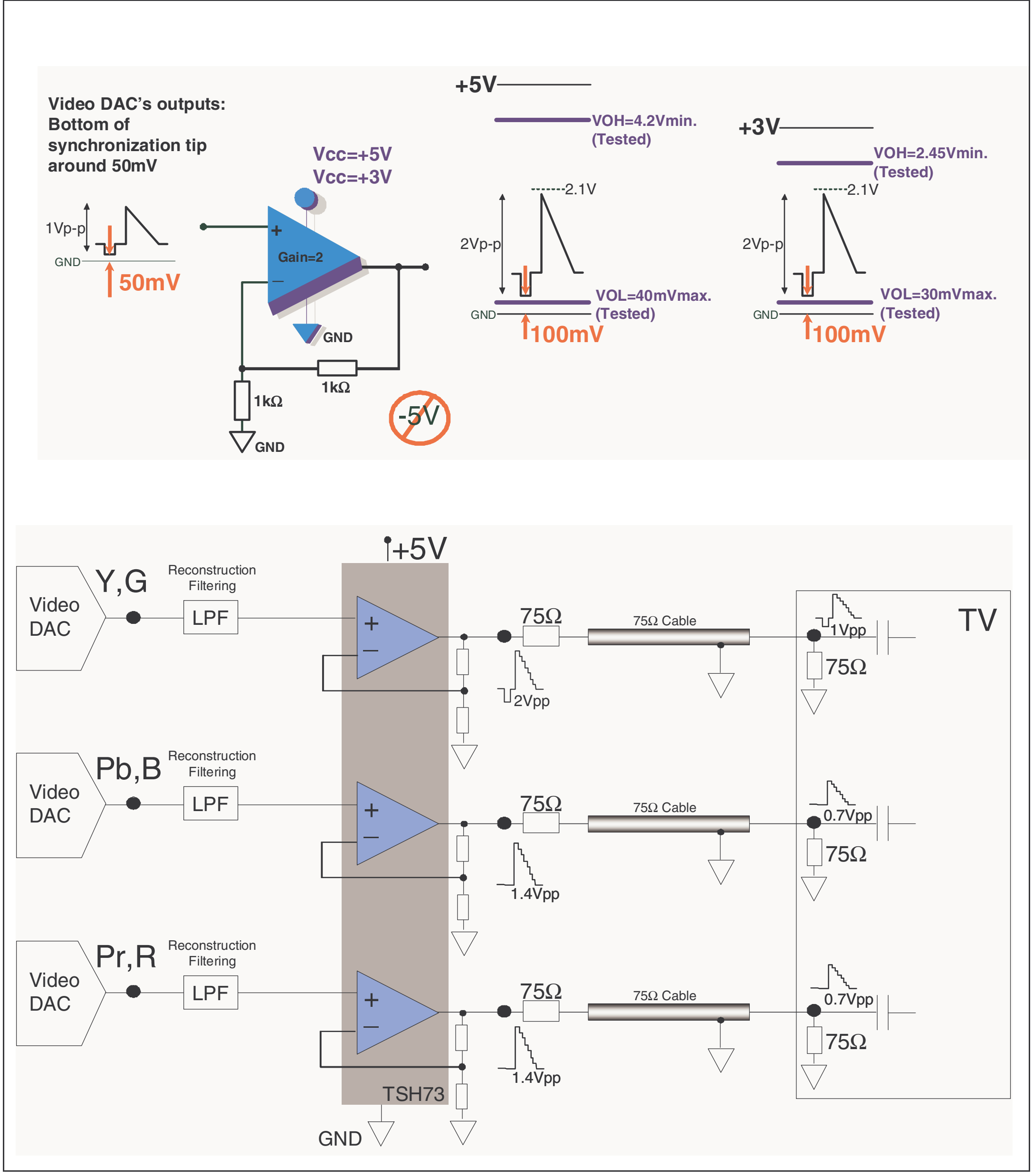
Part Number	Temperature Range	Package	Packing	Marking
TSH70CLT	0°C to 70°C	SOT23-5	Tape & Reel	K301
TSH70CD/CDT		SO-8	Tube or Tape & Reel	70C
TSH71CD/CDT		SO-8	Tube or Tape & Reel	71C
TSH71CPT		TSSOP8 (Thin Shrink Outline Package)	Tape & Reel	71C
TSH72CD/CDT		SO-8	Tube or Tape & Reel	72C
TSH72CPT		TSSOP8 (Thin Shrink Outline Package)	Tape & Reel	72C
TSH73CD/CDT		SO-14	Tube or Tape & Reel	73C
TSH73CPT		TSSOP14 (Thin Shrink Outline Package)	Tape & Reel	73C
TSH74CD/CDT		SO-14	Tube or Tape & Reel	74C
TSH74CPT		TSSOP14 (Thin Shrink Outline Package)	Tape & Reel	74C
TSH75CD/CDT		SO-16	Tube or Tape & Reel	75C
TSH75CPT		TSSOP16 (Thin Shrink Outline Package)	Tape & Reel	75C

2 Typical Application: Video Driver

A typical application for the TSH7x family is that of video driver for driving STi7xxx DAC outputs on 75-ohm lines.

Figure 1 show the benefits of the TSH7x family as single supply drivers.

Figure 1. Benefits of TSH7x family: +3V or +5V single supply solution



3 Absolute Maximum Ratings & Operating Conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (1)	14	V
V_{id}	Differential Input Voltage (2)	±2	V
V_i	Input Voltage (3)	±6	V
T_{oper}	Operating Free Air Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thjc}	Thermal resistance junction to case (4) SOT23-5 SO-8 SO-14 SO-16 TSSOPO8 TSSOP14 TSSOP16	 80 28 22 35 37 32 35	°C/W
R_{thja}	Thermal resistance junction to ambient area SOT23-5 SO-8 SO-14 SO-16 TSSOPO8 TSSOP14 TSSOP16	 250 157 125 110 130 110 110	°C/W
ESD	Human Body Model	2	kV

1. All voltages values, except differential voltage are with respect to network ground terminal
2. Differential voltages are non-inverting input terminal with respect to the inverting terminal
3. The magnitude of input and output must never exceed V_{CC} +0.3V
4. Short-circuits can cause excessive heating

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	3 to 12	V
V_{IC}	Common Mode Input Voltage Range	V_{CC}^- to (V_{CC}^+ -1.1)	V
Standby		(V_{CC}^-) to (V_{CC}^+)	V

4 Electrical Characteristics

Table 3. V_{CC}^+ = 3V, V_{CC}^- = GND, V_{IC} = 1.5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\|V_{io}\|$	Input Offset Voltage	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		1.2	10 12	mV
ΔV_{io}	Input Offset Voltage Drift vs. Temp.	$T_{min.} < T_{amb} < T_{max.}$		4		µV/°C
I_{io}	Input Offset Current	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		0.1	3.5 5	µA
I_{ib}	Input Bias Current	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		6	15 20	µA
C_{in}	Input Capacitance			0.2		pF
I_{CC}	Supply Current per Operator	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		7.2	9.8 11	mA
CMRR	Common Mode Rejection Ratio ($\delta V_{IC}/\delta Vio$)	$+0.1<V_{IC}<+1.9V$ & V_{out}=1.5V T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$	 65 64	 90		dB
SVRR	Supply Voltage Rejection Ratio ($\delta VCC/\delta Vio$)	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$	66 65	74		dB
PSRR	Power Supply Rejection Ratio ($\delta VCC/\delta V_{out}$)	Positive & Negative Rail		75		dB
A_{vd}	Large Signal Voltage Gain	R_L=150Ω to 1.5V, V_{out}=1V to 2V T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$	 70 65	 81		dB
I_o	Output Short Circuit Current Source	T_{amb}=25°C, V_{id}=+1, V_{out} to 1.5V, V_{id}=-1, V_{out} to 1.5V I_{Source} I_{Sink} $T_{min.} < T_{amb} < T_{max.}$ V_{id}=+1, V_{out} to 1.5V V_{id}=-1, V_{out} to 1.5V I_{Source} I_{Sink}	 30 20 22 19	 43 33		mA
V_{OH}	High Level Output Voltage	T_{amb}=25°C R_L = 150Ω to GND R_L = 600Ω to GND R_L = 2kΩ to GND R_L = 10kΩ to GND R_L = 150Ω to 1.5V R_L = 600Ω to 1.5V R_L = 2kΩ to 1.5V R_L = 10kΩ to 1.5V $T_{min.} < T_{amb} < T_{max.}$ R_L = 150Ω to GND R_L = 150Ω to 1.5V	 2.45 2.65 2.4 2.6	 2.60 2.87 2.91 2.93 2.77 2.90 2.92 2.93		V

Table 3. V_{CC}^{+} = 3V, V_{CC}^{-} = GND, V_{IC} = 1.5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage	T_{amb}=25°C R_L = 150Ω to GND R_L = 600Ω to GND R_L = 2kΩ to GND R_L = 10kΩ to GND R_L = 150Ω to 1.5V R_L = 600Ω to 1.5V R_L = 2kΩ to 1.5V R_L = 10kΩ to 1.5V $T_{min.} < T_{amb} < T_{max.}$ R_L = 150Ω to GND R_L = 150Ω to 1.5V		 10 11 11 11 140 90 68 57	 30 300 40 350	mV
GBP	Gain Bandwidth Product	F=10MHz A_{VCL}=+11 A_{VCL}=-10		 65 55		MHz
Bw	Bandwidth @-3dB	A_{VCL}=+1, R_L=150Ω to 1.5V		87		MHz
SR	Slew Rate	A_{VCL}=+2, R_L=150Ω // C_L to 1.5V C_L = 5pF C_L = 30pF	 45	 80 85		V/µs
φm	Phase Margin	R_L=150Ω // 30pF to 1.5V		40		°
en	Equivalent Input Noise Voltage	F=100kHz		11		nV/√Hz
THD	Total Harmonic Distortion	A_{VCL}=+2, F=4MHz, R_L=150Ω // 30pF to 1.5V V_{out}=1Vpp V_{out}=2Vpp		 -61 -54		dB
IM2	Second order intermodulation product	A_{VCL}=+2, V_{out}=2Vpp R_L=150Ω to 1.5V Fin1=180kHz, Fin2=280KHz spurious measurements @100kHz		-76		dBc
IM3	Third order inter modulation product	A_{VCL}=+2, V_{out}=2Vpp R_L=150Ω to 1.5V Fin1=180kHz, Fin2=280KHz spurious measurements @400kHz		-68		dBc
ΔG	Differential gain	A_{VCL}=+2, R_L=150Ω to 1.5V F=4.5MHz, V_{out}=2Vpp		0.5		%
Df	Differential phase	A_{VCL}=+2, R_L=150Ω to 1.5V F=4.5MHz, V_{out}=2Vpp		0.5		°
Gf	Gain Flatness	F=DC to 6MHz, A_{VCL}=+2		0.2		dB
Vo1/Vo2	Channel Separation	F=1MHz to 10MHz		65		dB

Table 4. $V_{CC}^+ = 5V$, $V_{CC}^- = GND$, $V_{IC} = 2.5V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\|V_{io}\|$	Input Offset Voltage	$T_{amb} = 25°C$ $T_{min.} < T_{amb} < T_{max.}$		1.1	10 12	mV
ΔV_{io}	Input Offset Voltage Drift vs. Temp.	$T_{min.} < T_{amb} < T_{max.}$		3		µV/°C
I_{io}	Input Offset Current	$T_{amb} = 25°C$ $T_{min.} < T_{amb} < T_{max.}$		0.1	3.5 5	µA
I_{ib}	Input Bias Current	$T_{amb} = 25°C$ $T_{min.} < T_{amb} < T_{max.}$		6	15 20	µA
C_{in}	Input Capacitance			0.3		pF
I_{CC}	Supply Current per Operator	$T_{amb} = 25°C$ $T_{min.} < T_{amb} < T_{max.}$		8.2	10.5 11.5	mA
CMRR	Common Mode Rejection Ratio ($\delta V_{IC}/\delta Vio$)	$+0.1<V_{IC}<3.9V$ & $V_{out}=2.5V$ $T_{amb} = 25°C$ $T_{min.} < T_{amb} < T_{max.}$	 72 71	 97		dB
SVRR	Supply Voltage Rejection Ratio ($\delta V_{CC}/\delta Vio$)	$T_{amb} = 25°C$ $T_{min.} < T_{amb} < T_{max.}$	68 67	75		dB
PSRR	Power Supply Rejection Ratio ($\delta V_{CC}/\delta V_{out}$)	Positive & Negative Rail		75		dB
A_{vd}	Large Signal Voltage Gain	$R_L=150\Omega$ to 1.5V, $V_{out}=1V$ to 4V $T_{amb} = 25°C$ $T_{min.} < T_{amb} < T_{max.}$	 75 70	 84		dB
I_o	Output Short Circuit Current Source	$T_{amb}=25°C$, $V_{id}=+1$, V_{out} to 1.5V, $V_{id}=-1$, V_{out} to 1.5V I_{Source} I_{Sink} $T_{min.} < T_{amb} < T_{max.}$ $V_{id}=+1$, V_{out} to 1.5V $V_{id}=-1$, V_{out} to 1.5V I_{Source} I_{Sink}	 35 33 34 32	 55 55		mA
V_{OH}	High Level Output Voltage	$T_{amb}=25°C$ $R_L = 150\Omega$ to GND $R_L = 600\Omega$ to GND $R_L = 2k\Omega$ to GND $R_L = 10k\Omega$ to GND $R_L = 150\Omega$ to 2.5V $R_L = 600\Omega$ to 2.5V $R_L = 2k\Omega$ to 2.5V $R_L = 10k\Omega$ to 2.5V $T_{min.} < T_{amb} < T_{max.}$ $R_L = 150\Omega$ to GND $R_L = 150\Omega$ to 2.5V	 4.2 4.5 4.1 4.4	 4.36 4.85 4.90 4.93 4.66 4.90 4.92 4.93		V

Table 4. $V_{CC}^{+} = 5V$, $V_{CC}^{-} = GND$, $V_{IC} = 2.5V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage	T_{amb}=25°C R_L = 150Ω to GND R_L = 600Ω to GND R_L = 2kΩ to GND R_L = 10kΩ to GND R_L = 150Ω to 2.5V R_L = 600Ω to 2.5V R_L = 2kΩ to 2.5V R_L = 10kΩ to 2.5V $T_{min.} < T_{amb} < T_{max.}$ R_L = 150Ω to GND R_L = 150Ω to 2.5V		 20 23 23 23 220 105 76 61	 40 400 60 450	mV
GBP	Gain Bandwidth Product	F=10MHz A_{VCL}=+11 A_{VCL}=-10		 65 55		MHz
Bw	Bandwidth @-3dB	A_{VCL}=+1, R_L=150Ω to 2.5V		87		MHz
SR	Slew Rate	A_{VCL}=+2, R_L=150Ω // C_L to 2.5V C_L = 5pF C_L = 30pF	 60	 104 105		V/μs
φm	Phase Margin	R_L=150Ω // 30pF to 2.5V		40		°
en	Equivalent Input Noise Voltage	F=100kHz		11		nV/√Hz
THD	Total Harmonic Distortion	A_{VCL}=+2, F=4MHz R_L=150Ω // 30pF to 2.5V V_{out}=1Vpp V_{out}=2Vpp		 -61 -54		dB
IM2	Second order intermodulation product	A_{VCL}=+2, V_{out}=2Vpp R_L=150Ω to 2.5V Fin1=180kHz, Fin2=280kHz spurious measurements @100kHz		-76		dBc
IM3	Third order inter modulation product	A_{VCL}=+2, V_{out}=2Vpp R_L=150Ω to 2.5V Fin1=180kHz, Fin2=280KHz spurious measurements @400kHz		-68		dBc
ΔG	Differential gain	A_{VCL}=+2, R_L=150Ω to 2.5V F=4.5MHz, V_{out}=2Vpp		0.5		%
Df	Differential phase	A_{VCL}=+2, R_L=150Ω to 2.5V F=4.5MHz, V_{out}=2Vpp		0.5		°
Gf	Gain Flatness	F=DC to 6MHz, A_{VCL}=+2		0.2		dB
Vo1/Vo2	Channel Separation	F=1MHz to 10MHz		65		dB

Table 5. V_{CC}^{+} = 5V, V_{CC}^{-} = -5V, V_{IC} = GND, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\|V_{io}\|$	Input Offset Voltage	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		0.8	10 12	mV
ΔV_{io}	Input Offset Voltage Drift vs. Temp.	$T_{min.} < T_{amb} < T_{max.}$		2		µV/°C
I_{io}	Input Offset Current	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		0.1	3.5 5	µA
I_{ib}	Input Bias Current	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		6	15 20	µA
C_{in}	Input Capacitance			0.7		pF
I_{CC}	Supply Current per Operator	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$		9.8	12.3 13.4	mA
CMRR	Common Mode Rejection Ratio ($\delta V_{IC}/\delta Vio$)	$-4.9<V_{IC}<3.9V$ & V_{out}=GND T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$	 81 80	 106		dB
SVRR	Supply Voltage Rejection Ratio ($\delta V_{CC}/\delta Vio$)	T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$	71 70	77		dB
PSRR	Power Supply Rejection Ratio ($\delta V_{CC}/\delta V_{out}$)	Positive & Negative Rail		75		dB
A_{vd}	Large Signal Voltage Gain	R_L=150Ω to GND V_{out}=-4 to +4 T_{amb} = 25°C $T_{min.} < T_{amb} < T_{max.}$	 75 70	 86		dB
I_o	Output Short Circuit Current Source	T_{amb}=25°C V_{id}=+1, V_{out} to 1.5V V_{id}=-1, V_{out} to 1.5V I_{Source} I_{Sink} $T_{min.} < T_{amb} < T_{max.}$ V_{id}=+1, V_{out} to 1.5V V_{id}=-1, V_{out} to 1.5V I_{Source} I_{Sink}	 35 30 34 29	 55 55		mA
V_{OH}	High Level Output Voltage	T_{amb}=25°C R_L = 150Ω to GND R_L = 600Ω to GND R_L = 2kΩ to GND R_L = 10kΩ to GND $T_{min.} < T_{amb} < T_{max.}$ R_L = 150Ω to GND	 4.2 4.1	 4.36 4.85 4.9 4.93		V
V_{OL}	Low Level Output Voltage	T_{amb}=25°C R_L = 150Ω to GND R_L = 600Ω to GND R_L = 2kΩ to GND R_L = 10kΩ to GND $T_{min.} < T_{amb} < T_{max.}$ R_L = 150Ω to GND		 -4.63 -4.86 -4.9 -4.93	 -4.4 -4.3	V

Table 5. V_{CC}^{+} = 5V, V_{CC}^{-} = -5V, V_{IC} = GND, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GBP	Gain Bandwidth Product	F=10MHz A_{VCL}=+11 A_{VCL}=-10		65 55		MHz
Bw	Bandwidth @-3dB	A_{VCL}=+1 R_L=150Ω // 30pF to GND		100		MHz
SR	Slew Rate	A_{VCL}=+2, R_L=150Ω // C_L to GND C_L = 5pF C_L = 30pF	 68	117 118		V/μs
φm	Phase Margin	R_L=150Ω to GND		40		°
en	Equivalent Input Noise Voltage	F=100kHz		11		nV/√Hz
THD	Total Harmonic Distortion	A_{VCL}=+2, F=4MHz R_L=150Ω // 30pF to GND V_{out}=1Vpp V_{out}=2Vpp		-61 -54		dB
IM2	Second order intermodulation product	A_{VCL}=+2, V_{out}=2Vpp R_L=150Ω to GND Fin1=180kHz, Fin2=280KHz spurious measurements @100kHz		-76		dBc
IM3	Third order intermodulation product	A_{VCL}=+2, V_{out}=2Vpp R_L=150Ω to GND Fin1=180kHz, Fin2=280KHz spurious measurements @400kHz		-68		dBc
ΔG	Differential gain	A_{VCL}=+2, R_L=150Ω to GND F=4.5MHz, V_{out}=2Vpp		0.5		%
Df	Differential phase	A_{VCL}=+2, R_L=150Ω to GND F=4.5MHz, V_{out}=2Vpp		0.5		°
Gf	Gain Flatness	F=DC to 6MHz, A_{VCL}=+2		0.2		dB
Vo1/Vo2	Channel Separation	F=1MHz to 10MHz		65		dB

4.1 Standby mode

Table 6. V_{CC}^+, V_{CC}^-, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{low}	Standby Low Level		V_{CC}^-		$(V_{CC}^- +0.8)$	V
V_{high}	Standby High Level		$(V_{CC}^- +2)$		(V_{CC}^+)	V
$I_{CC\ STBY}$	Current Consumption per Operator when STANDBY is Active	pin 8 (TSH71) to V_{CC}^- pin 1,2 or 3 (TSH73) to V_{CC}^- pin 8 (TSH75) to V_{CC}^+ pin 9 (TSH75) to V_{CC}^-		20	55	µA
Z_{out}	Output Impedance (R_{out}//C_{out})	R_{out} C_{out}		10 17		MΩ pF
T_{on}	Time from Standby Mode to Active Mode			2		µs
T_{off}	Time from Active Mode to Standby Mode	Down to $I_{CC\ STBY}$ = 10µA		10		µs

TSH71 STANDBY CONTROL pin 8 ($\overline{STBY}$)	OPERATOR STATUS
V_{low}	Standby
V_{high}	Active

TSH73 STANDBY CONTROL			OPERATOR STATUS		
pin 1 ($\overline{STBY}$ OP1)	pin 2 ($\overline{STBY}$ OP2)	pin 3 ($\overline{STBY}$ OP3)	OP1	OP1	OP3
V_{low}	x	x	Standby	x	x
V_{high}	x	x	Active	x	x
x	V_{low}	x	x	Standby	x
x	V_{high}		x	Active	x
x	x	V_{low}	x	x	Standby
x	x	V_{high}	x	x	Active

TSH75 STANDBY CONTROL		OPERATOR STATUS			
pin 8 (STBY OP2)	pin 9 ($\overline{STBY}$ OP3)	OP1	OP2	OP3	OP4
V_{high}	V_{low}	Active	Standby	Standby	Active
V_{high}	V_{high}	Active	Standby	Active	Active
V_{low}	V_{low}	Active	Active	Standby	Active
V_{low}	V_{high}	Active	Active	Active	Active

4.2 Characteristic curves for V_{CC}=3V

Figure 2. Closed loop gain and phase vs. frequency (Gain = +2, V_{CC} = ±1.5V, R_L = 150Ω, T_{amb} = 25°C)

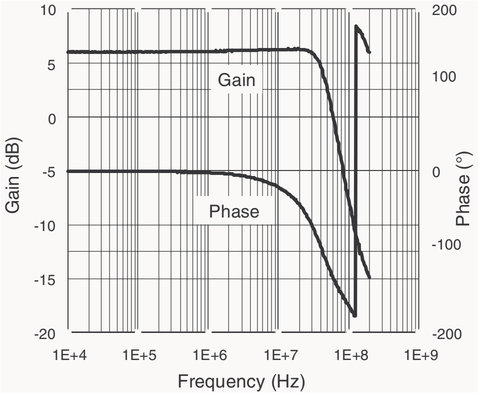


Figure 3. Overshoot function of output capacitance (Gain = +2, V_{CC} = ±1.5V, T_{amb} = 25°C)

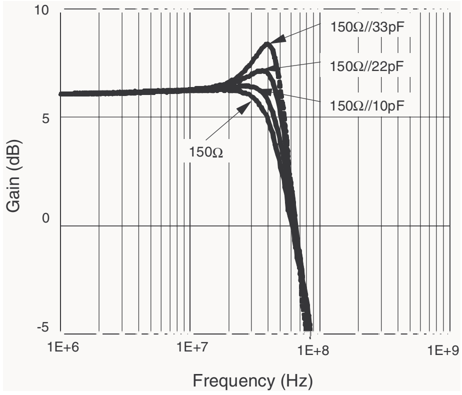


Figure 4. Closed loop gain and phase vs. frequency (Gain = -10, V_{CC} = ±1.5V, R_L = 150Ω, T_{amb} = 25°C)

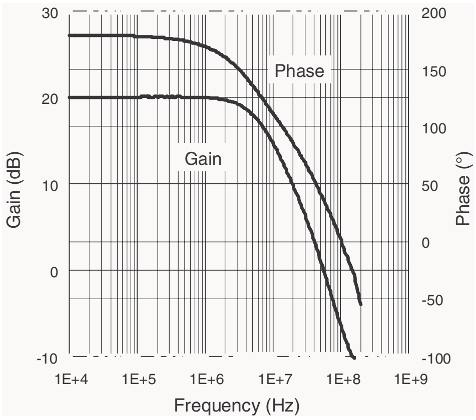


Figure 5. Closed loop gain and phase vs. frequency (Gain = +11, V_{CC} = ±1.5V, R_L = 150Ω, T_{amb} = 25°C)

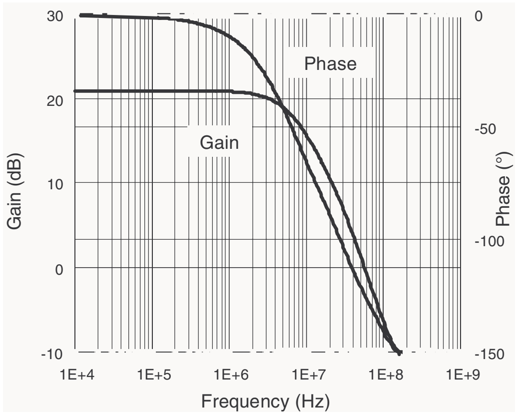


Figure 6. Large signal measurement - positive slew rate (Gain = 2, V_{CC} = ±1.5V, Z_L = 150Ω//5.6pF)

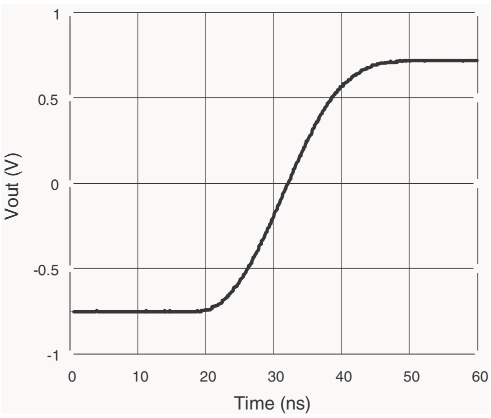


Figure 7. Large signal measurement - negative slew rate (Gain = 2, V_{CC} = ±1.5V, Z_L = 150Ω//5.6pF)

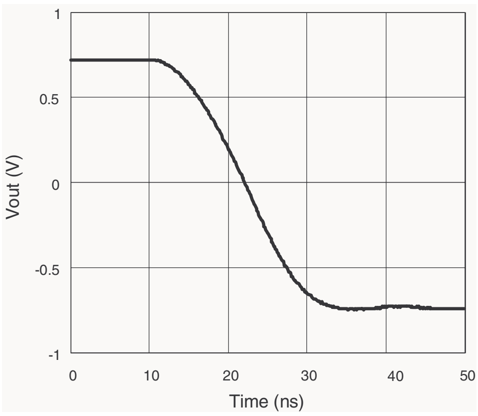


Figure 8. Small signal measurement - rise time (Gain = 2, V_{CC} = ±1.5V, Z_L = 150Ω)

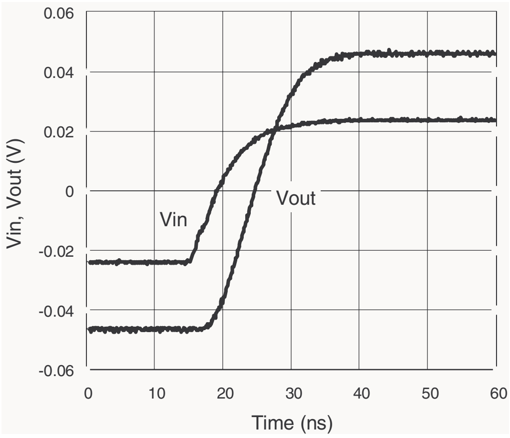


Figure 9. Small signal measurement - fall time (Gain = 2, V_{CC} = ±1.5V, Z_L = 150Ω)

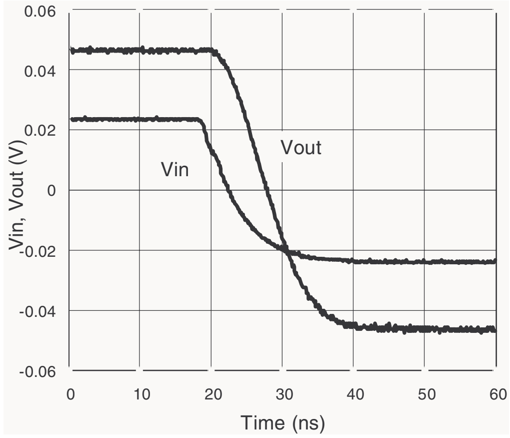


Figure 10. Channel separation (Xtalk) vs. frequency (measurement configuration: Xtalk = 20log (V0/V1))

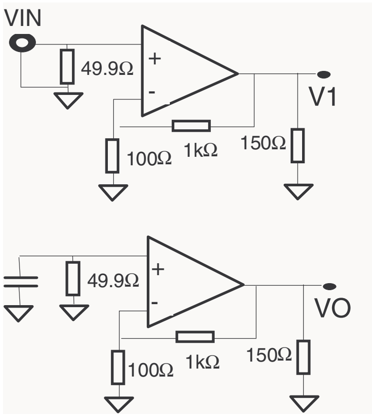


Figure 11. Channel separation (Xtalk) vs. frequency (Gain = +11, V_{CC} = 1.5V, Z_L = 150Ω//27pF)

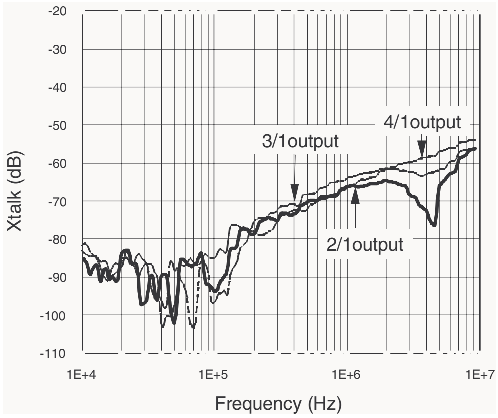


Figure 12. Equivalent noise voltage (Gain = 100, V_{CC} = ±1.5V, No load)

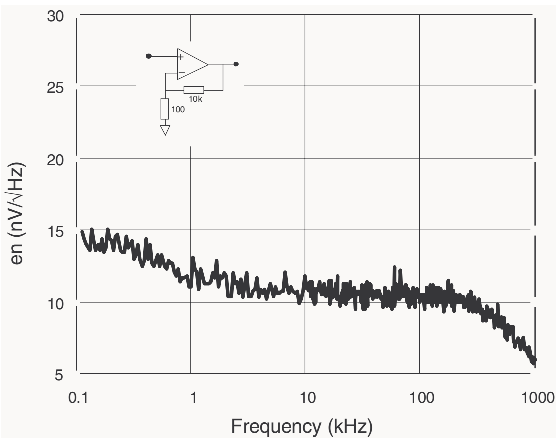


Figure 13. Maximum output swing (Gain = 11, V_{CC} = ±5V, R_L = 150Ω)

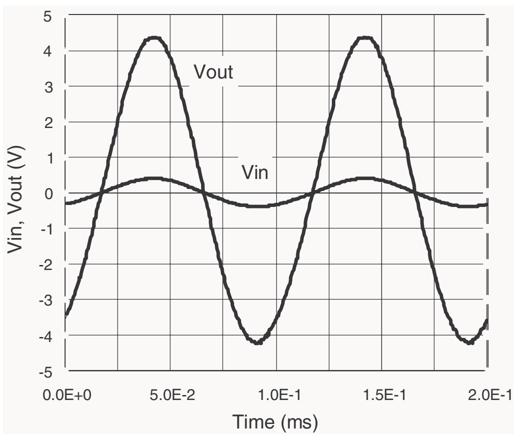


Figure 14. Standby mode - T_{on}, T_{off} (V_{CC} = ±1.5V, open loop)

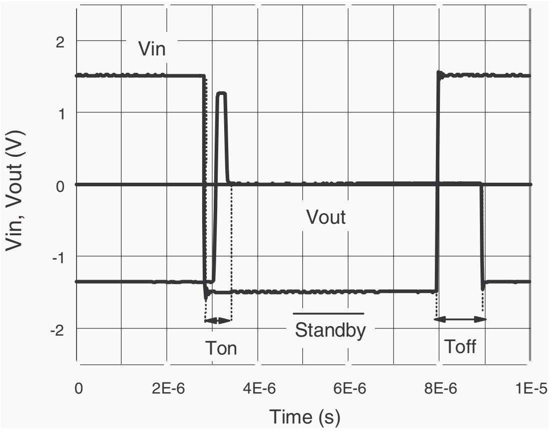


Figure 15. Group delay gain = 2 (V_{CC} = ±1.5V, Z_L = 150Ω//27pF, T_{amb} = 25°C)

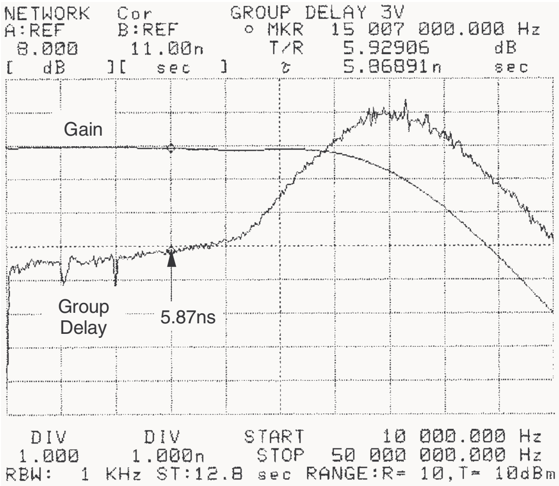
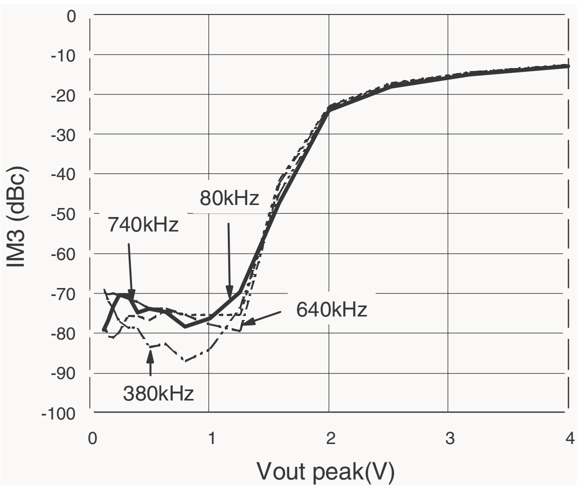


Figure 16. Third order intermodulation(1) (Gain = 2, V_{CC} = ±1.5V, Z_L = 150Ω//27pF, T_{amb} = 25°C)



1. Note on intermodulation products:
   The IFR2026 synthesizer generates a two tones signal (F1=180kHz, F2=280kHz); each tone having the same amplitude level.
   The HP3585 spectrum analyzer measures the intermodulation products function of the output voltage.
   The generator and the spectrum analyzer are phase locked for precision considerations.

4.3 Characteristic curves for V_{CC}=5V

Figure 17. Closed loop gain and phase vs. frequency (Gain = +2, V_{CC} = ±2.5V, R_L = 150Ω, T_{amb} = 25°C)

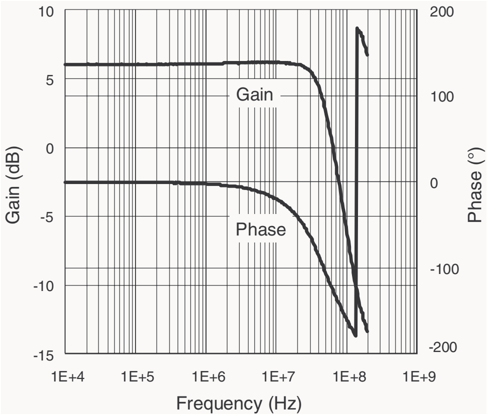


Figure 18. Overshoot function of output capacitance (Gain = +2, V_{CC} = ±2.5V, T_{amb} = 25°C)

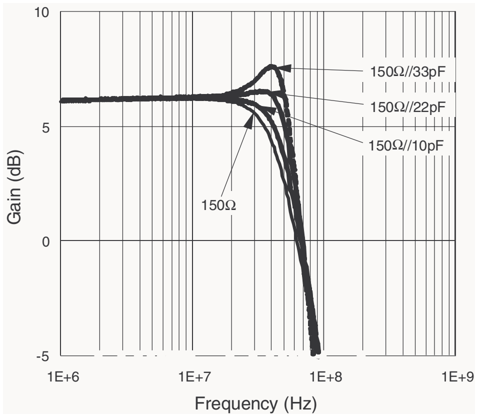


Figure 19. Closed loop gain and phase vs. frequency (Gain = -10, V_{CC} = ±2.5V, R_L = 150Ω, T_{amb} = 25°C)

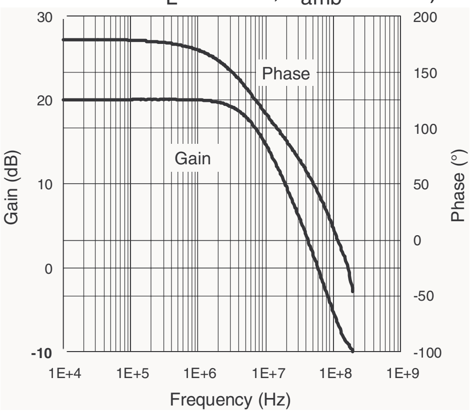


Figure 20. Closed loop gain and phase vs. frequency (Gain = +11, V_{CC} = ±2.5V, R_L = 150Ω, T_{amb} = 25°C)

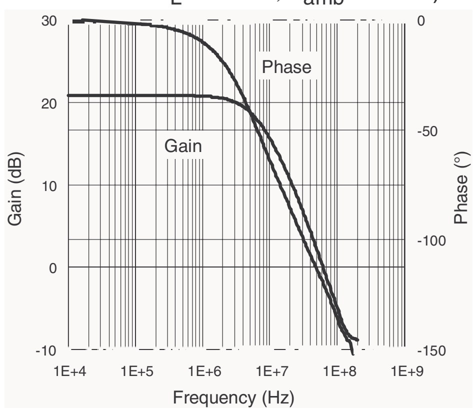


Figure 21. Large signal measurement - positive slew rate (Gain = 2, V_{CC} = ±2.5V, Z_L= 150Ω//5.6pF)

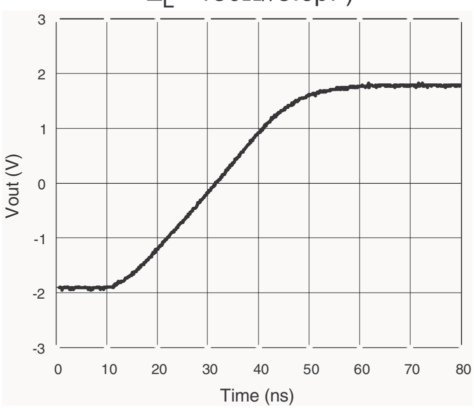


Figure 22. Large signal measurement - negative slew rate (Gain = 2, V_{CC} = ±2.5V, Z_L = 150Ω//5.6pF)

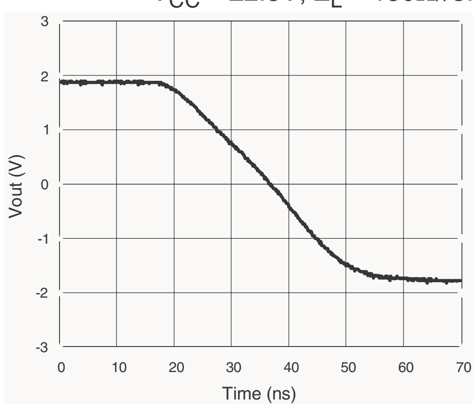


Figure 23. Small signal measurement - rise time (Gain = 2, V_{CC} = ±2.5V, Z_L = 150Ω)

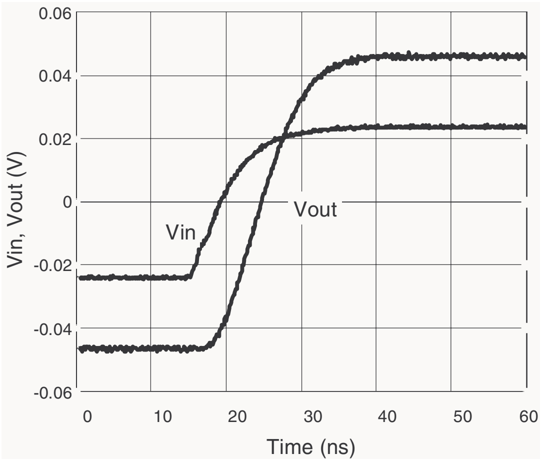


Figure 24. Small signal measurement - fall time (Gain = 2, V_{CC} = ±2.5V, Z_L= 150Ω)

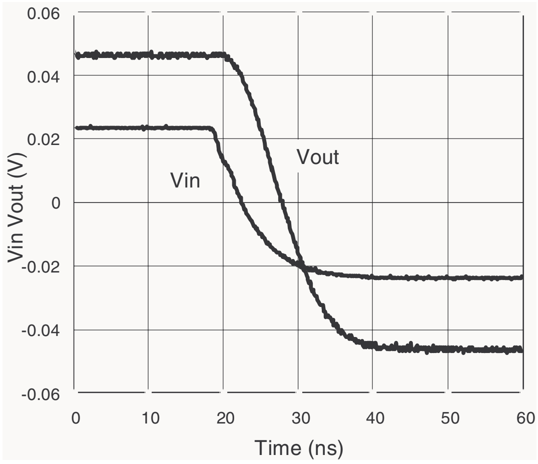


Figure 25. Channel separation (Xtalk) vs. frequency (measurement configuration: Xtalk = 20log (V0/V1))

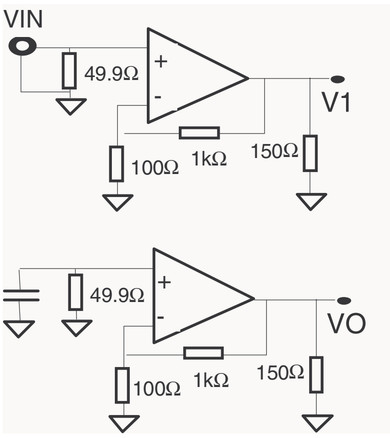


Figure 26. Channel separation (Xtalk) vs. frequency (Gain = +11, V_{CC} = ±2.5V, Z_L = 150Ω//27pF)

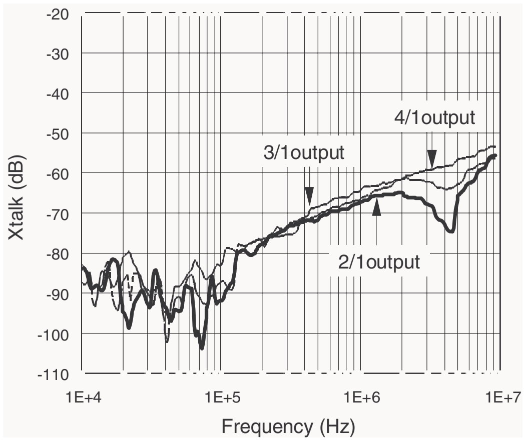


Figure 27. Equivalent noise voltage (Gain = 100, V_{CC} = ±2.5V, no load)

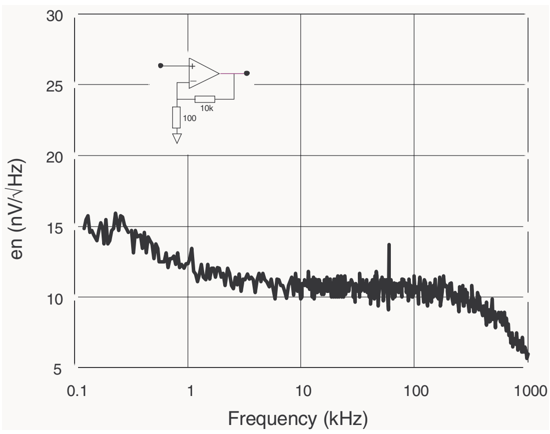


Figure 28. Maximum output swing (Gain = 11, V_{CC} = ±2.5V, R_L = 150Ω)

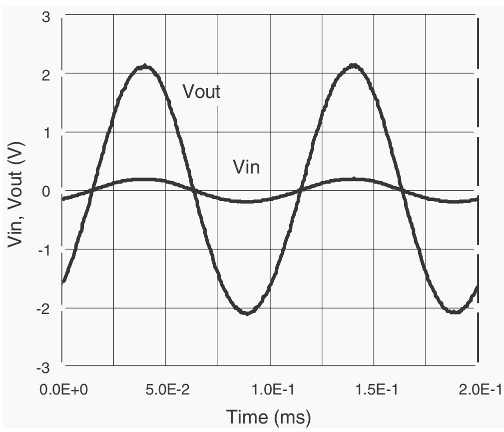


Figure 29. Standby mode - T_{on}, T_{off} (V_{CC} = ±2.5V, open loop)

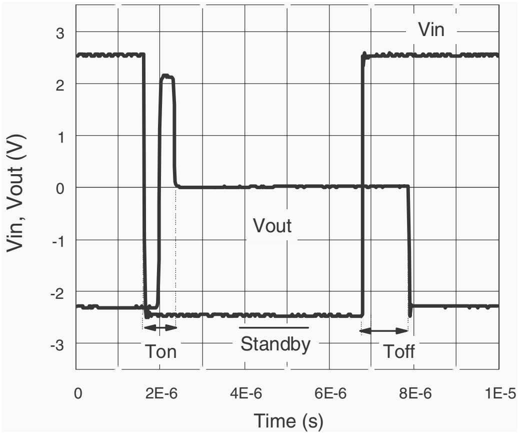


Figure 30. Group delay (Gain = 2, V_{CC} = ±2.5V, Z_L = 150Ω//27pF, T_{amb} = 25°C)

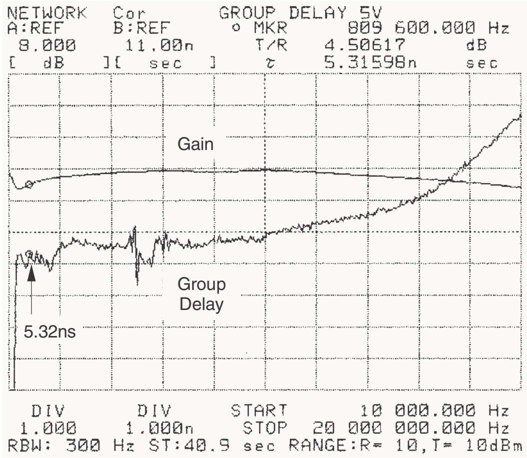
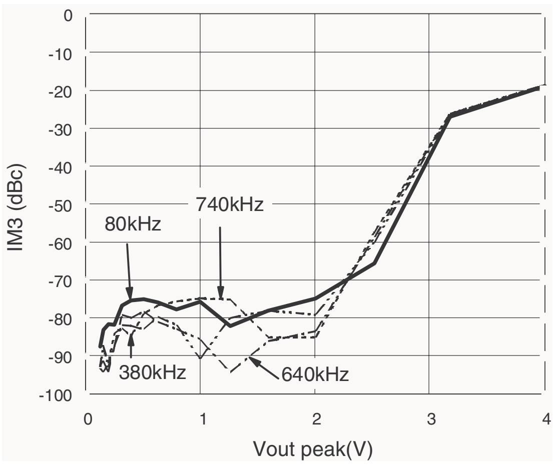


Figure 31. Third order intermodulation[(1)] (Gain = 2, V_{CC} = ±2.5V, Z_L = 150Ω//27pF, T_{amb} = 25°C)



1. Note on intermodulation products:
The IFR2026 synthesizer generates a two tones signal (F1=180kHz, F2=280kHz); each tone having the same amplitude level.
The HP3585 spectrum analyzer measures the intermodulation products function of the output voltage.
The generator and the spectrum analyzer are phase locked for precision considerations.

4.4 Characteristic curves for V_{CC}=10V

Figure 32. Closed loop gain and phase vs. frequency (Gain = +2, V_{CC} = ±5V, R_L = 150Ω, T_{amb} = 25°C)

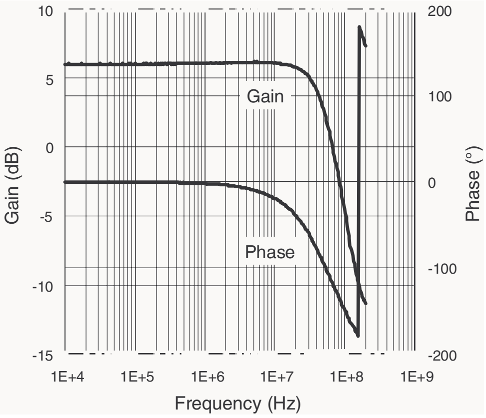


Figure 33. Overshoot function of output capacitance (Gain = +2, V_{CC} = ±5V, T_{amb} = 25°C)

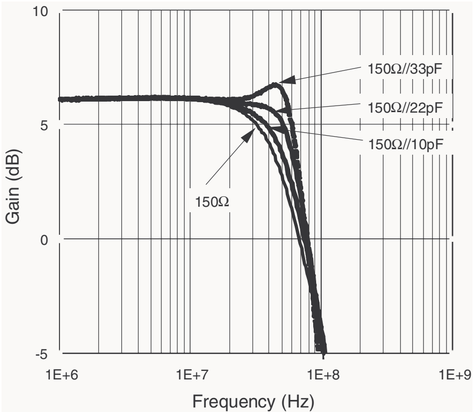


Figure 34. Closed loop gain and phase vs. frequency (Gain = -10, V_{CC} = ±5V, R_L = 150Ω, T_{amb} = 25°C)

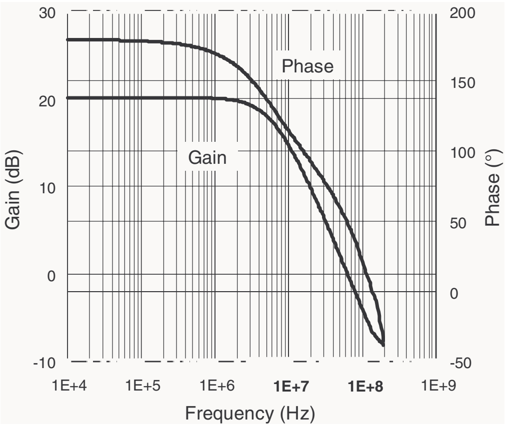


Figure 35. Closed Loop Gain and Phase vs. Frequency (Gain = +11, V_{CC} = ±5V, R_L = 150Ω, T_{amb} = 25°C)

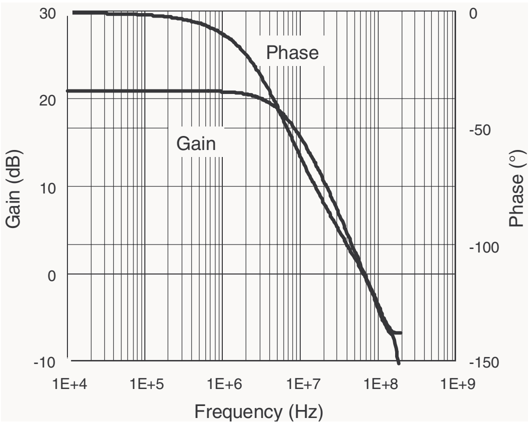


Figure 36. Large signal measurement - positive slew rate (Gain = 2,V_{CC} = ±5V, Z_L = 150Ω//5.6pF)

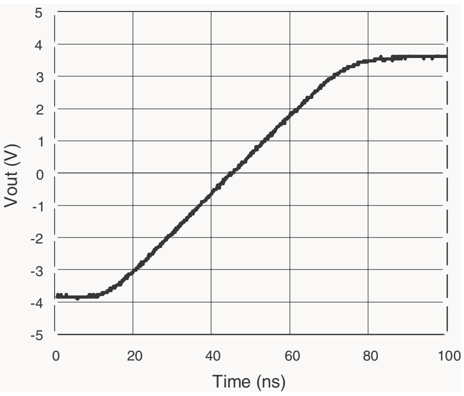


Figure 37. Large Signal Measurement - Negative Slew Rate (Gain = 2 V_{CC} = ±5V, Z_L = 150Ω//5.6pF)

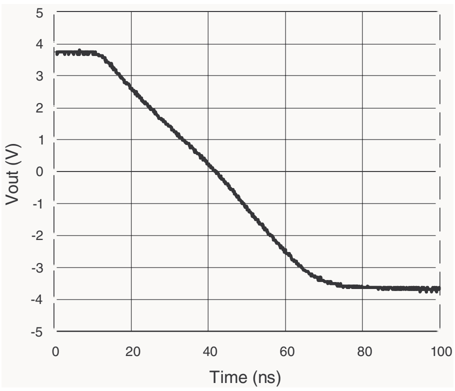


Figure 38. Small signal measurement - rise time (Gain = 2, V_{CC} = ±5V, Z_L = 150Ω)

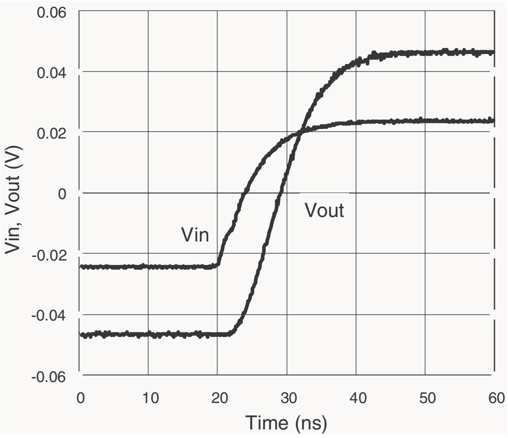


Figure 39. Small signal measurement - fall time (Gain = 2, V_{CC} = ±5V, Z_L = 150Ω)

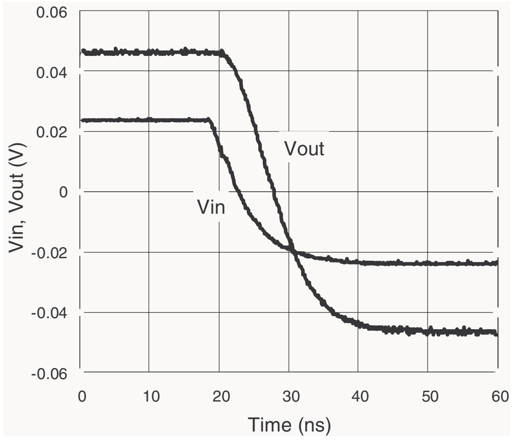


Figure 40. Channel separation (Xtalk) vs. frequency (measurement configuration: Xtalk = 20log(V0/V1))

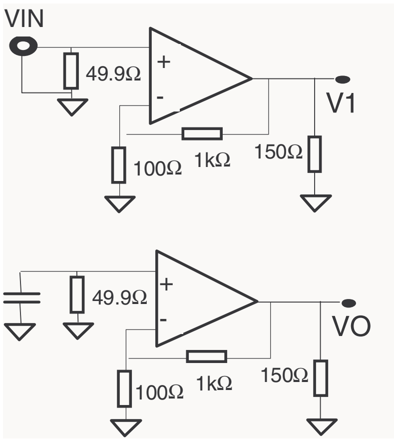


Figure 41. Channel separation (Xtalk) vs. frequency (Gain = +11, V_{CC} = ±5V, Z_L = 150Ω//27pF)

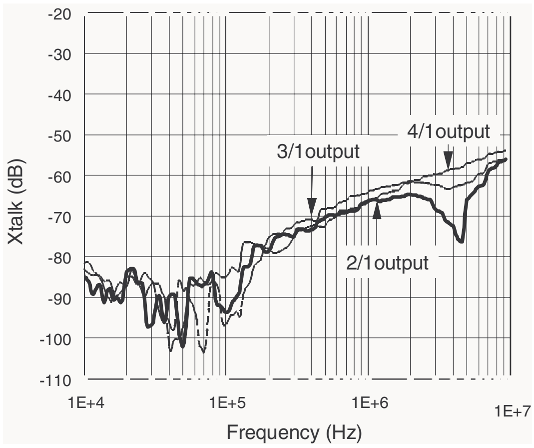


Figure 42. Equivalent noise voltage (Gain =100, V_{CC} = ±5V, no load)

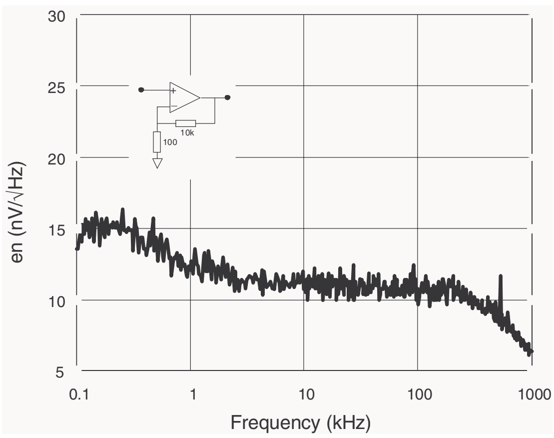


Figure 43. Maximum output swing (Gain = 11, V_{CC} = ±5V, R_L = 150Ω)

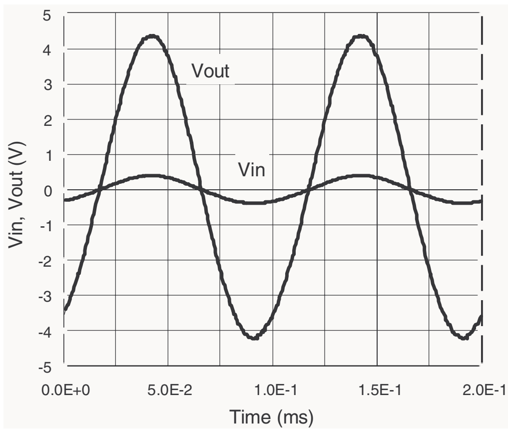


Figure 44. Standby mode - T_{on}, T_{off} (V_{CC} = ±5V, open loop)

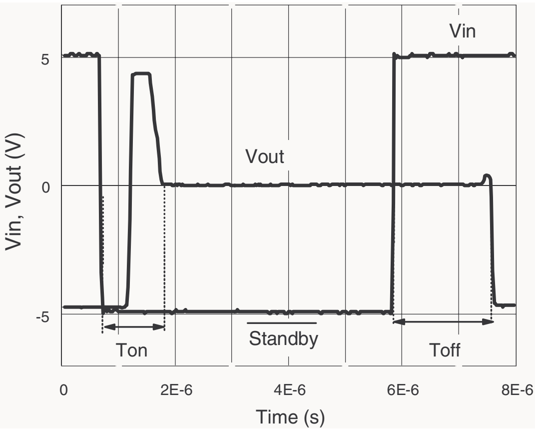


Figure 45. Group Delay (Gain = 2, V_{CC}= ±5V Z_L = 150Ω//27pF, T_{amb} = 25°C)

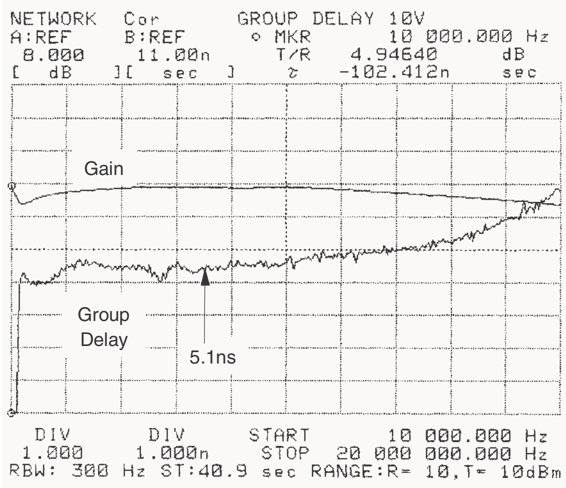
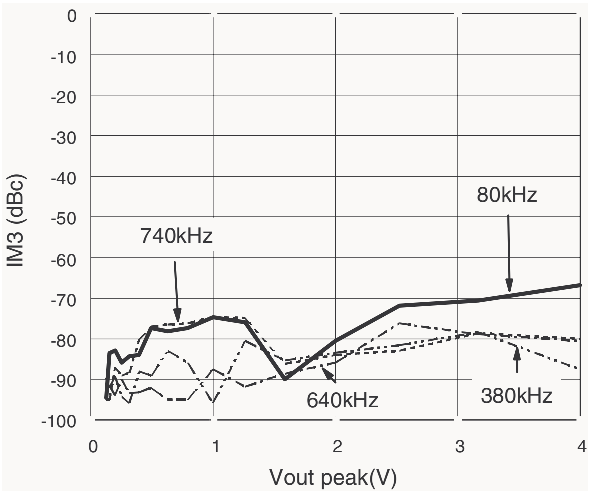


Figure 46. Third order intermodulation[1] (Gain = 2, V_{CC} = ±5V, Z_L = 150Ω//27pF, T_{amb} = 25°C



1. Note on intermodulation products:
The IFR2026 synthesizer generates a two tones signal (F1=180kHz, F2=280kHz); each tone having the same amplitude level.
The HP3585 spectrum analyzer measures the intermodulation products function of the output voltage.
The generator and the spectrum analyzer are phase locked for precision considerations.

5 Testing Conditions

5.1 Layout precautions

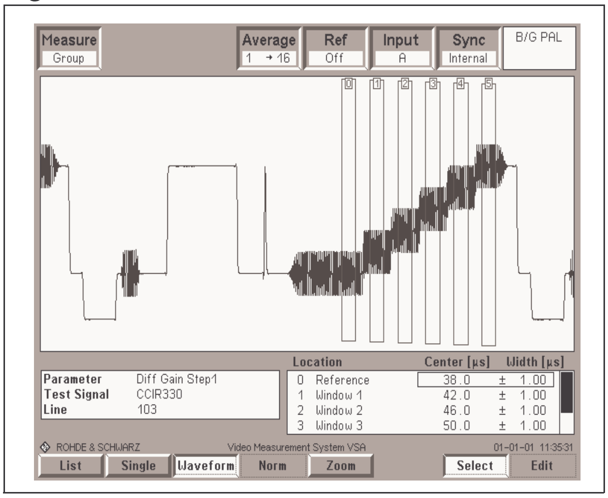
To use the TSH7X circuits in the best manner at high frequencies, some precautions have to be taken for power supplies:

- First of all, the implementation of a proper ground plane in both sides of the PCB is mandatory for high speed circuit applications to provide low inductance and low resistance common return.
- Power supply bypass capacitors (4.7uF and ceramic 100pF) should be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion. The power supply capacitors must be incorporated for both the negative and the positive pins.

- Proper termination of all inputs and outputs must be in accordance with output termination resistors; in this way, the amplifier load will be resistive only, and the stability of the amplifier will be improved.
- All leads must be wide and as short as possible (especially for op-amp inputs and outputs) in order to decrease parasitic capacitance and inductance.
- For lower gain applications, care should be taken to avoid large feedback resistance (>1kΩ) in order to reduce the time constant of parasitic capacitances.
- Choose component sizes as small as possible (SMD).
- Finally, on output, the load capacitance must be negligible to maintain good stability. You can put a serial resistance as close as possible to the output pin to minimize capacitance.

5.2 Maximum input level

Figure 47. CCIR330 video line



The input level must not exceed the following values:

- negative peak: must be greater than $-V_{CC}$+400mV.
- positive peak value: must be lower than $+V_{CC}$-400mV.

The electrical characteristics show the influence of the load on this parameter.

5.3 Video capabilities

To characterize the differential phase and differential gain, a CCIR330 video line is used.

The video line contains 5 (flat) levels of luma on which is superimposed chroma signal. The first level contains no luma. The luma gives various amplitudes which define the saturation of the signal. The chrominance gives various phases which define the color of the signal.

Differential phase (respectively differential gain) distortion is present if a signal chrominance phase (gain) is affected by luminance level. They represent the ability to uniformly process the high frequency information at all luminance levels.

When differential gain is present, color saturation is not correctly reproduced.

The input generator is the Rohde & Schwarz CCVS. The output measurement was done by the Rohde and Schwarz VSA.

Figure 48. Measurement on Rohde and Schwarz VSA

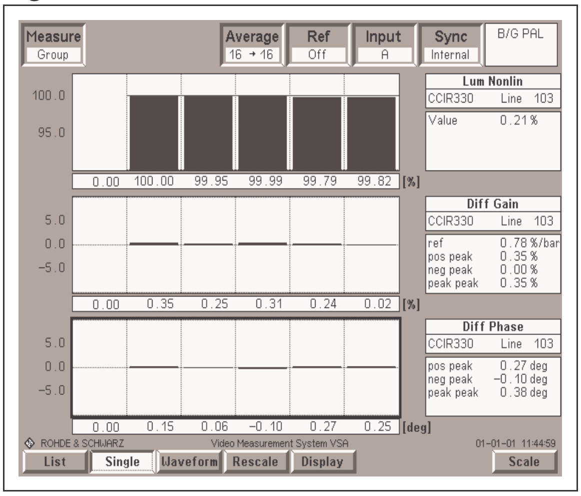


Table 7. Video results

Parameter	Value $V_{CC} = \pm2.5V$	Value $V_{CC} = \pm5V$	Unit
Lum NL	0.1	0.3	%
Lum NL Step 1	100	100	%
Lum NL Step 2	100	99.9	%
Lum NL Step 3	99.9	99.8	%
Lum NL Step 4	99.9	99.9	%
Lum NL Step 5	99.9	99.7	%
Diff Gain pos	0	0	%
Diff Gain neg	-0.7	-0.6	%
Diff Gain pp	0.7	0.6	%

Table 7. Video results

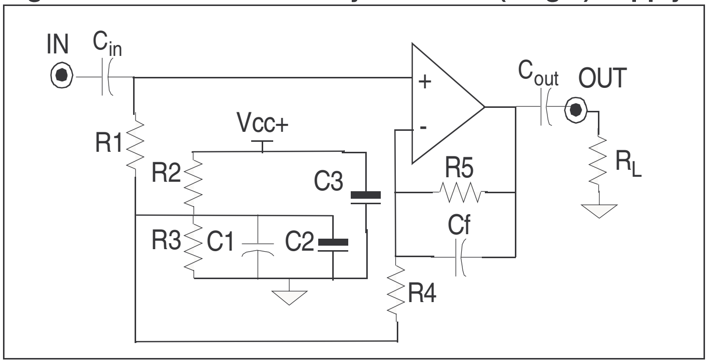
Parameter	Value $V_{CC} = \pm2.5V$	Value $V_{CC} = \pm5V$	Unit
Diff Gain Step1	-0.5	-0.3	%
Diff Gain Step2	-0.7	-0.6	%
Diff Gain Step3	-0.3	-0.5	%
Diff Gain Step4	-0.1	-0.3	%
Diff Gain Step5	-0.4	-0.5	%
Diff Phase pos	0	0.1	deg
Diff Phase neg	-0.2	-0.4	deg
Diff Phase pp	0.2	0.5	deg
Diff Phase Step1	-0.2	-0.4	deg
Diff Phase Step2	-0.1	-0.4	deg
Diff Phase Step3	-0.1	-0.3	deg
Diff Phase Step4	0	0.1	deg
Diff Phase Step5	-0.2	-0.1	deg

5.4 Precautions when operating on an asymmetrical supply

The TSH7X can be used with either a dual or a single supply. If a single supply is used, the inputs are biased to the mid-supply voltage ($+V_{CC}/2$). This bias network must be carefully designed, in order to reject any noise present on the supply rail.

As the bias current is 15uA, you must carefully choose the resistance R1 so as not to introduce an offset mismatch at the amplifier inputs.

Figure 49. Schematic of asymmetrical (single) supply

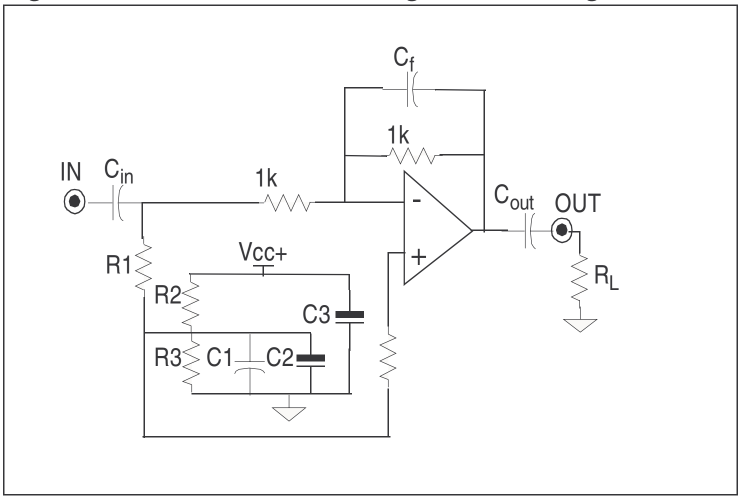


R1 = 10KΩ is a typical and convenient value. C1, C2, C3 are bypass capacitors that filter perturbations on V_{CC}, as well as for the input and output signals. We choose C1 = 100nF and C2 = C3 = 100uF.

R2, R3 are such that the current through them must be greater than 100 times the bias current. Therefore, we set R2 = R3 = 4.7KΩ.

C_{in}, as C_{out}, is chosen to filter the DC signal by the low-pass filters (R1,C_{in} and R_{out}, C_{out}). By taking R1 = 10KΩ, R_L = 150Ω, and C_{in} = 2uF, C_{out}=220uF we provide a cut-off frequency below 10Hz.

Figure 50. Use of the TSH7x in gain = -1 configuration



Some precautions must be taken, especially for low-power supply applications.

A feedback capacitance, C_f, should be added for better stability. *Table 8* summarizes the impact of the capacitance C_f on the phase margin of the circuit.

Table 8. Impact capacitance C_f

Parameter	C_f (pF)	$V_{CC} = \pm 1.5V$	$V_{CC} = \pm 2.5V$	$V_{CC} = \pm 5V$	Unit
Phase Margin	0	28	43	56	deg
f-3dB		40	39.3	38.3	MHz
Phase Margin	5.6	30	43	56	deg
f-3dB		40	39.3	38.3	MHz
Phase Margin	22	37	52	67	deg
f-3dB		37	34	32	MHz
Phase Margin	33	48	65	78	deg
f-3dB		33.7	30.7	27.6	MHz

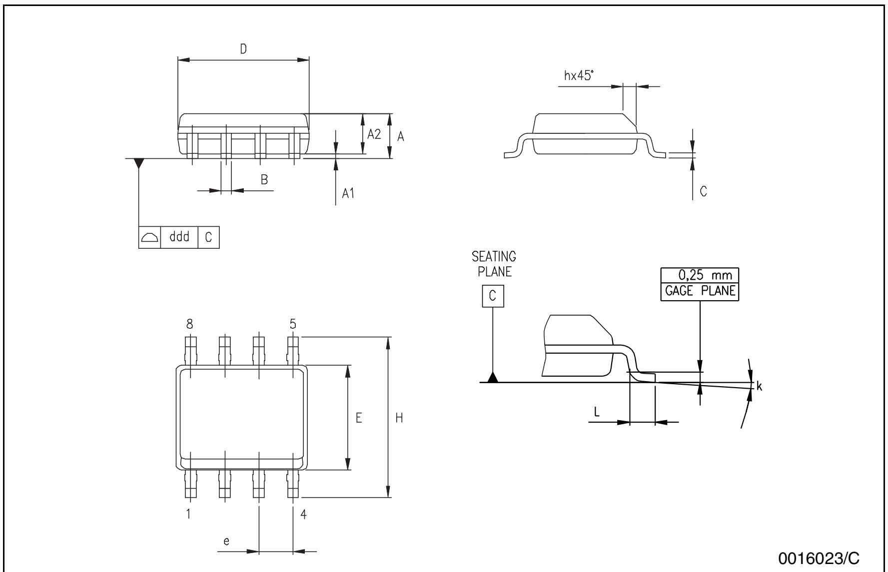
6 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

6.1 SO-8 Package

SO-8 MECHANICAL DATA

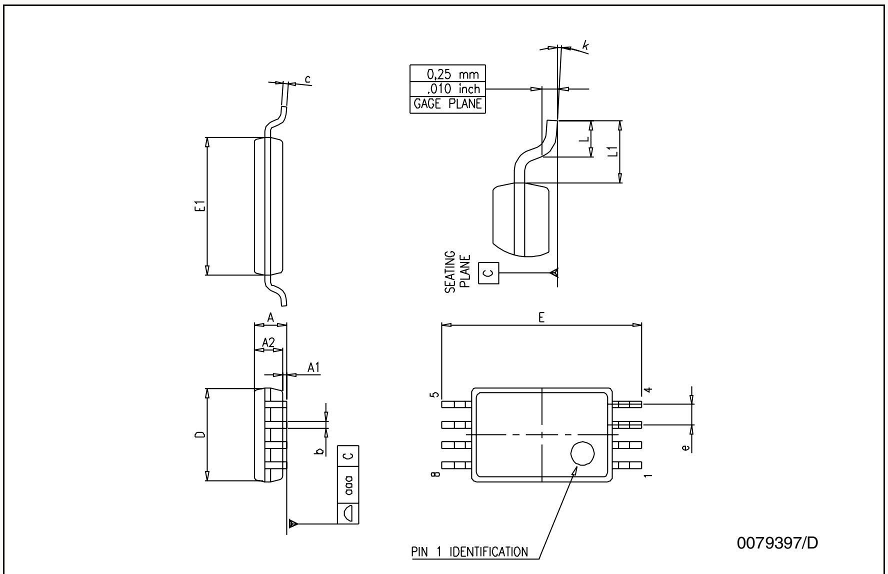
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



6.2 TSSOP8 Package

TSSOP8 MECHANICAL DATA

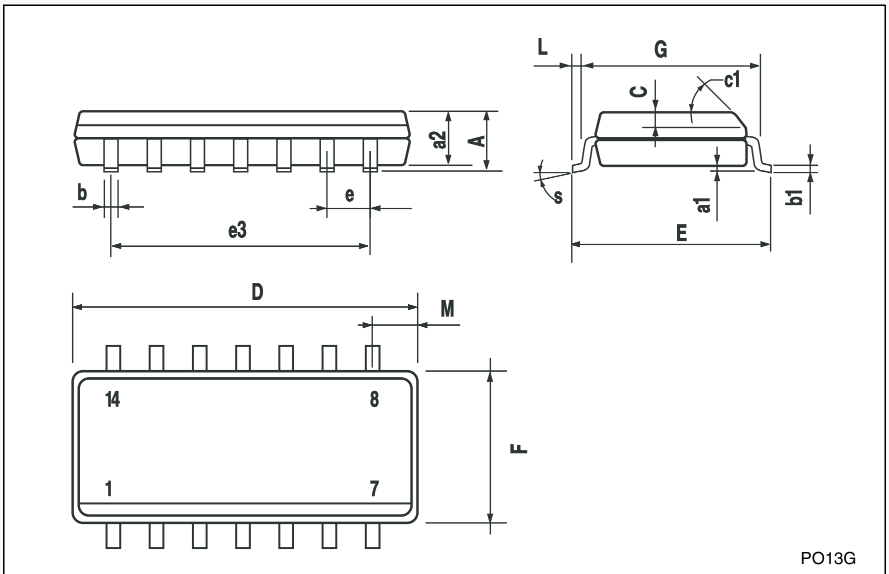
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0˚		8˚	0˚		8˚
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	



6.3 SO-14 Package

SO-14 MECHANICAL DATA

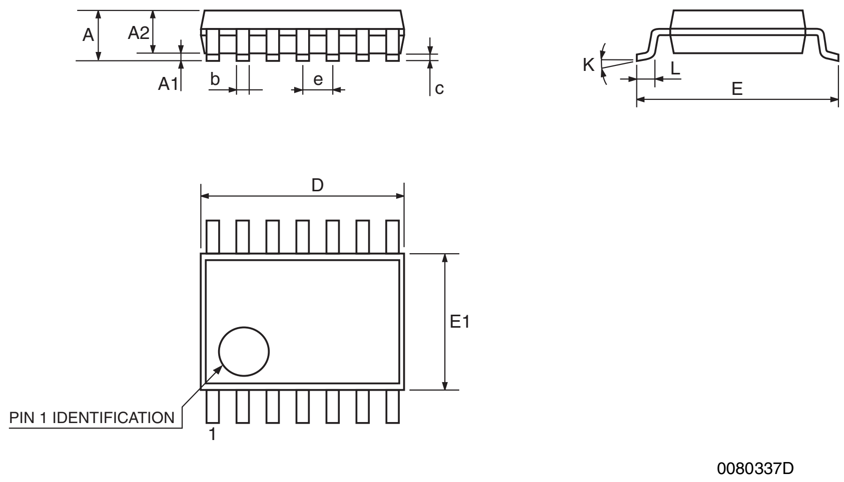
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45˚ (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8˚ (max.)					



6.4 TSSOP14 Package

TSSOP14 MECHANICAL DATA

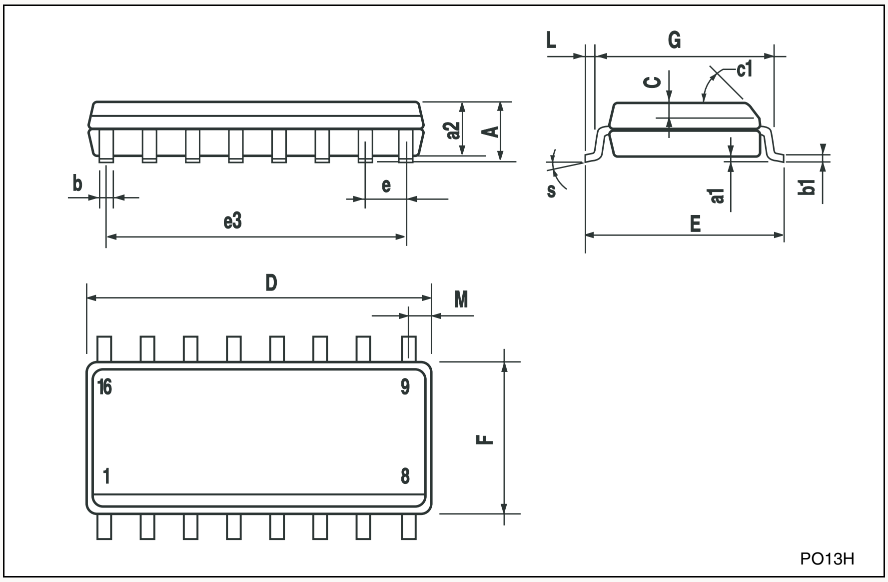
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



6.5 SO-16 Package

SO-16 MECHANICAL DATA

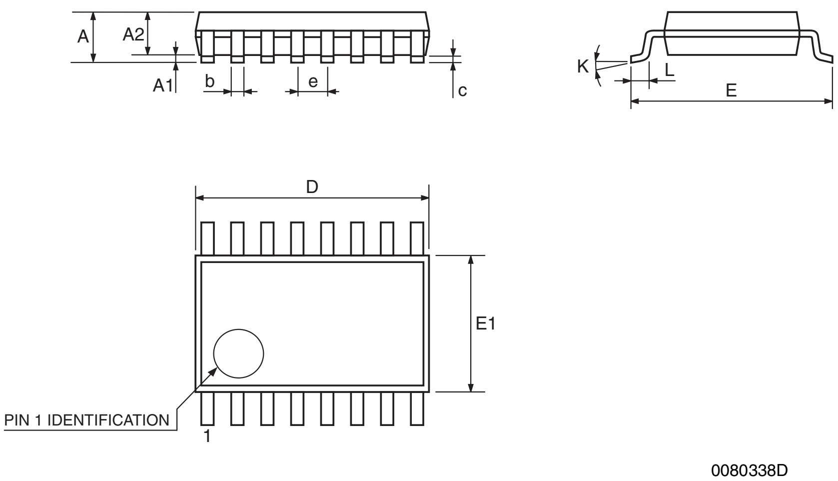
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.008
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 ° (max.)					



6.6 TSSOP16 Package

TSSOP16 MECHANICAL DATA

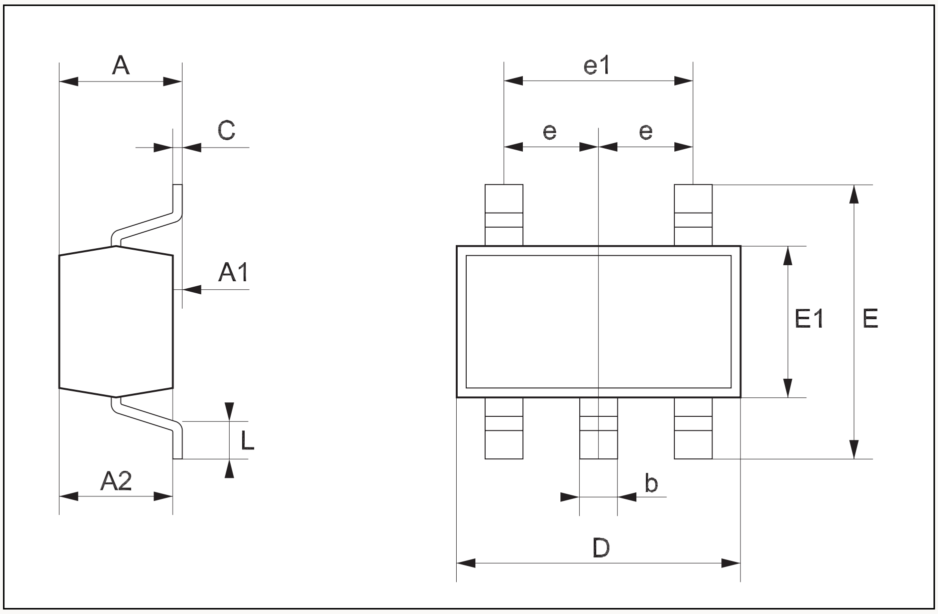
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



6.7 SOT23-5 Package

SOT23-5L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6



7 Revision History

Table 9. Document revision history

Date	Revision	Changes
Nov. 2000	1	First Release.
Aug. 2002	2	Limit min. of I_{sink} from 24mA to 20mA (only on 3V power supply). Reason: yield improvement.
May 2006	3	Improvement of VOL max. at 3V and 5V power supply on 150-ohm load connected to GND (pages 6 and 8). Reason: TSH7x can drive video signals from DACs to lines in single supply (3V or 5V) without any DC level change of the video signals. Grammatical and typographical changes throughout. Package mechanical data updated.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com